Amendments to the Specification:

Please replace the title at page 1, line 1, with the following amended title:

METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE ~~AND MANUFACTURING METHOD THEREOF~~

Please add the following new paragraph after the title at page 1, line 2:

This application is a divisional of Application Serial No. 09/714,891 filed November 17, 2000, now U.S. Patent No. 6,646,287.

Please replace the paragraph bridging pages 5 and 6, with the following amended paragraph:

In order to form an LDD region having an ~~above-descibed~~ above-described concentration gradient of an impurity element, a method of doping into a semiconductor layer is used, in which an ionized impurity element for controlling conductivity is accelerated by an electric field, and made to pass through a portion of the gate electrode and a gate insulating film (a gate insulating film formed between the gate electrode and the semiconductor layer, and in close contact with both, and an insulating film extending in a region in the periphery of the gate insulating film, is included in the term gate insulating film for the present invention). In addition, the gate electrode is tapered so that the thickness thereof gradually increases from an edge portion of the gate electrode toward the inside, and concentration of the impurity element doped into the semiconductor layer is controlled by utilizing that change in thickness. Namely, the LDD region is formed so that the concentration of the impurity element gradually changes toward the longitudinal direction of the TFT channel.

Please replace the paragraph beginning at page 16, line 15, with the following amended paragraph:

The resist [[1009]] 1007 is then used as a mask, and a first doping process is performed. A single conductivity type impurity element is added to the island-like semiconductor layer 1003. An ion doping method or an ion injection method in which the impurity element is ionized, accelerated by an electric field, and then injected into the semiconductor layer is performed as the doping process. The single conductivity type impurity element passes through the gate insulating film and is added to the semiconductor layer beneath. A portion of the single conductivity type impurity element can be added to the semiconductor layer passing through an edge portion and the vicinity of the conductive layer 1008 having the first tapered shape.

Please replace the paragraph beginning at page 17, line 6, with the following amended paragraph:

An enlarged view of a region [[1017]] 1013 surrounded by a dotted line in Fig. 1B is shown in Figs. 2A-1. Further, Figs. 2A-2 is a diagram which schematically expresses the concentration distribution of the impurity element in arbitrary units. The impurity region is formed under the gate insulating film and the tapered portion of the gate electrode. The concentration distribution of the impurity element is shown by a line 1030, and decreases with the distance from the first impurity region 1011. The ratio of the decrease differs depending on the acceleration voltage and the dosage amount during ion doping, and with an angle θ1 of the tapered portion and the thickness of the first shape gate electrode 1008.

Please replace the paragraph bridging pages 18 and 19 with the following amended paragraph:

The second impurity region (B) 1018 is formed under the second shape gate insulating film 1016 and [[nuder]] under the tapered portion of the second tapered shape conductive layer 1015. Its concentration distribution of the impurity element is shown by a line 1031, and decreases with a distance from the first impurity region 1011. The second tapered shape conductive layer 1015 is used as a gate electrode. By making the edge portion of the gate electrode having a tapered shape, and by doping the impurity element through the tapered portion, an impurity region can thus be formed in the semiconductor layer existing under the tapered portion in which the concentration of the impurity element changes gradually. The present invention actively utilizes this impurity region. By forming this type of impurity region, a high electric field developing in the vicinity of the drain region is relieved, then the deterioration of the TFT can be prevented because of generation of hot carriers.

Please replace the paragraph beginning at page 19, line 8, with the following amended paragraph:

Thus the first impurity region 1026 which becomes a source region or a drain region, the second impurity region (A) which forms the LDD region 1025 not overlapping the gate electrode, the second impurity region (B) which forms the LDD region 1024 overlapping a portion of the gate electrode, and a channel forming region 1023 are formed in the island-like semiconductor layer 1003. Then, when necessary, an interlayer insulating film 1020 may be formed, and a wiring 1021 which contacts with the source region or the drain region may be formed, as shown in Fig. 1D.

Please replace the paragraph bridging pages 21 and 22, with the following amended paragraph:

A crystallization process is then performed, and a crystalline semiconductor layer 103b is manufactured from the amorphous semiconductor layer 103a. Laser annealing, thermal annealing (solid state growth method), and rapid thermal annealing (RTA method) can be applied as the crystallization method. When using a glass substrate such as those stated above, or a plastic substrate with inferior heat resistance, it is particular preferable to apply laser annealing. An light source such as an infrared lamp, a halogen lamp, a metal halide lamp, or a xenon lamp is used by the RTA method. Alternatively, the crystalline semiconductor layer 103b can be formed by a crystallization method using a catalytic element, in accordance with a technique disclosed by Japanese Patent Application Laid-open No. Hei. 7-130652. In this crystallization process, first it is preferable to release hydrogen contained in the amorphous semiconductor layer, and if ~~thecrystallization~~ the crystallization is performed after the amount of hydrogen contained is made equal to or less than 5 atom% by performing heat treatment at 400 to 500EC for approximately 1 hour, then roughness of the film surface can be prevented.

Please replace the paragraph bridging pages 24 and 25, with the following amended paragraph:

A heat resistant conductive layer 111 for forming a gate electrode is then formed with a thickness of 200 to 400 nm (preferably between 250 and 350 nm) on the first shape gate insulating film 109, as shown in Fig. 3D. The heat resistant conductive layer may be formed by a single layer and may also be a lamination structure composed of a plurality of layers such as a two layers or three layers structure, when necessary. In this specification, the heat resistant conductive layer contains an element chosen from the group consisting of Ta, Ti, W and Mo or an alloy of the above elements, or an alloy film of a combination of said elements. These heat resistant conductive layers are formed by sputtering or CVD, and it is preferable to reduce the impurity element concentration

contained in order to make the resistance low. In particular, it is preferable to make the concentration of oxygen equal to or less than 30 ppm. A 300 nm thick W film is formed in Embodiment 1. The W film may be formed by sputtering with W as a target, and can also be formed by thermal CVD using tungsten hexafluoride (WF_6). Whichever is used, it is necessary to be able to make the film become low resistance in order to use as the gate electrode, and it is preferable that the resistivity of the W film be made equal to or less than 20 [[Ωcm]] μΩcm. The resistivity can be lowered by enlarging the crystals of the W film, but for cases in which there are a many impurity elements such as oxygen within the W film, crystallization is inhibited, and the film becomes high resistance. Thus a W target having a purity of 99.9999% is used in sputtering, and by additionally forming the W film taking sufficient care so as not to introduce any impurities from within the gas phase at the time of film deposition, a resistivity of 9 to 20 [[Ωcm]] μΩcm can be achieved.

Please replace the paragraph bridging pages 25 and 26, with the following amended paragraph:

When using a Ta film in the heat resistant conductive layer, it is possible to form the Ta film similarly by sputtering. Ar is used in the sputtering gas for the Ta film. Further, if an appropriate amount of Xe and Kr are added to the gas at the time of sputtering, then the internal stress of the film formed is relaxed, and film peeling can be prevented. The resistivity of an α phase Ta film is on the order of 20 [[Ωcm]] μΩcm, and it can be used in the gate electrode, but the resistivity of a [[α]] β phase Ta film is on the order of 180 [[Ωcm]] μΩcm and it is unsuitable for the gate electrode. A TaN film possesses a crystal structure which is close to that of α phase Ta film, and therefore an α phase Ta film can easily be obtained provided that a TaN film is formed under the Ta film. Further, although not shown in the figures, it is effective to form a silicon film doped by phosphorous (P) and having a thickness on the order of 2 to 20 nm under the heat

resistant conductive layer 111. By doing that increasing the adhesion and preventing oxidation of the conductive film formed on top, at the same time alkaline metal elements contained in the heat resistant conductive layer 111 in microscopic amounts can be stopped from diffusing into the first shape gate insulating film 109 by doing so. Whichever is used, it is preferable that the resistivity of the heat resistant conductive layer 111 be in a range from 10 to 50 [[Ωcm]] μΩcm.

Please replace the paragraph beginning at page 33, line 5, with the following amended paragraph:

In the first n-channel TFT 201, a conductive layer having the second tapered shape functions as a gate electrode 221. The structure of the island-like semiconductor layer 105 has a channel forming region 208, a first impurity region 209a which functions as a source region or a drain region, a second impurity region (A) 209b which forms an LDD region not overlapping the gate electrode 221, and a second impurity region (B) 209c which forms an LDD region overlapping a portion of the gate electrode 221. The length of the portion in which the second impurity region (B) 209c overlaps the gate electrode 221 is set from 0.1 to 0.3 [[·]] μm with respect to a channel length of 2 to 7 [[·]] μm. This length Lov is controlled by the thickness of the gate electrode 221 and by the angle of the tapered portion. By forming this type of LDD region in an n-channel TFT, the high electric field which develops near the drain region is relieved, and the development of hot carriers is blocked, then deterioration of the TFT can be prevented.

Please replace the paragraph bridging pages 33 and 34, with the following amended paragraph:

In the second n-channel TFT 203 of the driver circuit, a conductive layer having the second tapered shape functions as a gate electrode 223. The structure of the

island-like semiconductor layer 107 has a channel forming region 212, a first impurity region 213a which functions as a source region or a drain region, a second impurity region (A) 213b which forms an LDD region not overlapping the gate electrode 223, and a second impurity region (B) 213c which forms an LDD region overlapping a portion of the gate electrode 223. The length of the portion in which the second impurity region (B) 213c overlaps the gate electrode 223 is set similar to that of the second n-channel TFT 201, from 0.1 to 0.3 [[·]] μm.

Please replace the paragraph bridging pages 34 and 35, with the following amended paragraph:

In the pixel TFT 204 of the driver circuit, a conductive layer having the second tapered shape functions as a gate electrode 224. The structure of the island-like semiconductor layer 108 has channel forming regions 214a and 214b, first impurity region 215a and 217 which function as source regions or drain regions, a second impurity region (A) 215b which forms an LDD region not overlapping the gate electrode 224, and a second impurity region (B) 215c which forms an LDD region overlapping a portion of the gate electrode 224. The length of the portion in which the second impurity region (B) 213c overlaps the gate electrode 224 is set from 0.1 to 0.3 [[·]] μm. Further, a storage capacitor is formed from: a semiconductor layer which extends from the first impurity region 217 and has a second impurity region (A) 219b, a second impurity region (B) 219c, and a region 218 to which is not added impurity elements determining the conductivity type; an insulating layer formed by the same layer as the gate insulating film having the third shape; and a capacitor wiring 225 formed from the second tapered shape conductive layer.

Please replace the paragraph beginning at page 35, line 4, with the following amended paragraph:

Fig. 11 is a top view showing approximately one pixel of the pixel portion. A cross section along the line [[A-A□]] A-A' shown in the figure corresponds to the cross sectional diagram of the pixel portion shown in Fig. 5B. In the pixel TFT 204, a gate electrode 224 intersects, through a gate insulating film not shown in the figure, with the island-like semiconductor layer 108 formed below and stretches over a plurality of island-like semiconductor layers furthermore to serve as the gate wiring. Although not shown in the figure, a source region, a drain region, and an LDD region are formed in the island-like semiconductor layers, as explained by Fig. 5B. Further, reference numeral 230 denotes a contact portion of the source wiring 164 and the source region 215a, reference numeral 231 denotes a contact portion of the pixel electrode 169 and a drain region 217. The storage capacitor 205 is formed by a region in which the semiconductor layer extending from the drain region 217 of the pixel TFT 204 and the capacitor wiring 225 overlap, through the gate insulating film. An impurity element for controlling valence electrons is not added in the semiconductor layer 218 in this structure.

Please replace the paragraph bridging pages 36 and 37, with the following amended paragraph:

For a case of an active matrix type liquid crystal display device, the first p-channel TFT 200 and the first n-channel TFT 201 are used to form circuits such as a shift register circuit, a buffer circuit, and a level shifter circuit which place importance on high speed operation. In Fig. 5B, these circuits are denoted as a logic circuit portion. The second impurity region (B) 209c of the first n-channel TFT 201 becomes a structure which places importance on counteracting hot carriers. In addition, in order to increase voltage resistance and stabilize operation, the TFTs of the logic circuit portion may also be formed by a first p-channel TFT 280 and a first n-channel TFT 281, as shown by Fig.

9A. These TFTs have a double gate structure in which two gate electrodes are formed between one source and drain pair, and this type of TFT can be similarly manufactured by using the processes of Embodiment 1. The structure of the first p-channel TFT 280 has channel forming regions 236a and 236b, third impurity regions 238a, 239a, and 240a which function as source or drain regions, fourth impurity regions (A) 238b, 239b, and 240b which become LDD regions, and fourth impurity regions (B) 238c, 239c, and 240c which become LDD regions overlapping a portion of a gate electrode 237 in the island-like semiconductor layer. The structure of the first n-channel TFT 281 has channel forming regions 241a and 241b, first impurity regions 243a, 244a, and 245a which function as source or drain regions, second impurity regions (A) 243b, 244b, and 245b which become LDD regions, and second impurity regions (B) 243c, 244c, and 245c which become LDD regions overlapping a portion of a gate electrode 242 in the island-like semiconductor layer. Taking the length of the LDD region which overlaps the gate electrode as Lov, its length in the longitudinal direction of the channel is set from 0.1 to 0.3 [[·]] μm with respect to a channel length of 3 to 7 [[·]] μm.

Please replace the paragraph beginning at page 37, line 3, with the following amended paragraph:

Further, in a sampling circuit structured by analog switches, similarly structured second p-channel TFTs 202 and second n-channel TFTs 203 can be applied. The sampling circuit places importance on measures against hot carriers and low Off current operation therefore the TFT of this circuit may be formed by a second p-channel TFT 282 and a second n-channel TFT 283 as shown by Fig. 9B. The second p-channel TFT 282 has a triple gate structure in which three gate electrodes are formed between one source and drain pair, and this type of TFT can be similarly manufactured by using the processes of Embodiment 1. The structure of the second p-channel TFT 282 has channel forming regions 246a, 246b, and 246c, third impurity regions 249a, 250a, 251a,

and 252a which function as source or drain regions, fourth impurity regions (A) 249b, 250b, 251b, and 252b which become LDD regions, and fourth impurity regions (B) 249c, 250c, 251c, and 252c which become LDD regions overlapping a portion of a gate electrode 247. The structure of the second n-channel TFT 283 has channel forming regions 253a and 253b, first impurity regions 255a, 256a, and 257a which function as source or drain regions, second impurity regions (A) 255b, 256b, and 257b which become LDD regions, and second impurity regions (B) 255c, 256c, and 257c which become LDD regions overlapping a portion of a gate electrode 254. Taking the length of the LDD region which overlaps the gate electrode as Lov, its length in the longitudinal direction of the channel is set from 0.1 to 0.3 [[·]] μm with respect to a channel length of 3 to 7 [[·]] μm.

Please replace the paragraph beginning at page 40, line 9, with the following amended paragraph:

Thereafter, similar to Embodiment 1, by forming the second interlayer insulating film 159 made of an organic insulating material, source wirings 160 to 164, and drain wirings 165 to 168, pixel electrodes 169 and 171, the active matrix substrate can thus be completed. Figs. 7(A) and 7(B) show top views of this state, and the cross sections taken along the line [[B-B□]] B-B' of Fig. 7A and the line [[C-C□]] C-C' of Fig. 7B correspond to the [[B-B□]] B-B' and [[C-C□]] C-C' cross sections, respectively, in Fig. 5C. Although the gate insulating film, the first interlayer insulating film, and the second interlayer insulating film are omitted from the Figs. 7(A) and 7(B), the source and drain regions of the island semiconductor layers 104, 105, and 108 not shown in the figure are connected to the source wirings 160, 161 and 164, and drain wirings 165, 166 and the pixel electrode 169 through contact holes. Further, the cross sections taken along the line [[D-D□]] D-D' of Fig. 7A and the line [[E-E□]] E-E' of Fig. 7B are shown in Figs. 8A and 8B, respectively. The gate wiring 173 is formed overlapping the gate electrodes

220, and the gate wiring 174 is formed overlapping the gate electrode 225 in the outside of the island semiconductor layers 104 and 108. Thus, the gate electrode and the low-resistant conductive layer are in close contact to be electrically communicated without contact holes. By forming the gate wiring from a low-resistant conductive material in this way, the wiring resistance can be sufficiently reduced. Accordingly, the present invention can be applied to a display device that has a pixel portion (screen size) of 4-inch class or more.

Please replace the paragraph at page 53, line 2, with the following amended paragraph:

Note that the structure of this Embodiment can be readily realized by manufacturing the TFT in accordance with the steps shown in Embodiments 1 through 3. The structures of the pixel portion and the driver circuits only are shown in this embodiment. Other circuits such as a signal divider circuit, a frequency dividing circuit, a D/A converter, a [[_]] g correction circuit, an op-amp circuit, and further signal processing circuits such as a memory circuit and a processing circuit, and still further a logic circuit, may all be formed on the same substrate in accordance with the processes of Embodiments 1 through 3. In this way, the present invention can realize a semiconductor device comprising a pixel portion and a driver circuit thereof on the same substrate, for example, a liquid crystal display device equipped with a signal controlling circuit and a pixel portion.

Please replace the paragraph at page 54, line 15, with the following amended paragraph:

A glass plate, an aluminum plate, a stainless steel plate, an FRP (fiberglass-reinforced plastics) plate, a PVF (polyvinyl fluoride) film, a Mylar film (a product of

DUPONT Corp.), a polyester film, and an acrylic film or acrylic plate can be used as the counter substrate 80. A sheet having a structure in which several ten [[_m]] mm thick aluminum foil is interposed between a PVF film and a Mylar film, is used to enhance resistance to moisture. In this manner, the EL element is completely sealed and is not exposed to the outside of air.

Please replace the paragraph bridging pages 59 and 60, with the following amended paragraph:

Reference numeral 43 denotes a pixel electrode (cathode of an EL element) that is made of a conductive film with high reflectivity and is electrically connected to the drain of the current controlling TFT 2403. As the pixel electrode 43, a low resistant conductive film such as an aluminum alloy film, a copper alloy film, and a silver alloy film, or a lamination film thereof can be preferably used. Needless to say, a lamination structure with other conductive films may also be used. A light-emitting layer 44 is formed in a groove (corresponding to a pixel) formed by banks 44a and 44b made of an insulating film (preferably resin). Herein, only one pixel is shown, however, light-emitting layers corresponding to each color R (red), G (green), and B (blue) may be formed. As an organic EL material for the light-emitting layer, a ~~□conjugate~~ p-conjugate polymer material is used. Examples of the typical polymer material include polyparaphenylene vinylene (PPV), polyvinyl carbazole (PVK), and polyfluorene. There are various types of PPV organic EL materials. For example, materials as described in [[□H.]] "H. Shenk, Becker, O. Gelsen, E. Kluge, W. Kreuder and H. Spreitzer, ~~□Polymers~~ "Polymers for Light Emitting ~~Diodes□,~~ Diodes", Euro Display, Proceedings, 1999, pp. ~~33-37□~~ 33-37" and Japanese Laid-Open Publication No. 10-92576 can be used.